REMARKS

Present Status of Patent Application

Claims 10-18 remain pending of which claims 10 and 13 has been amended and claims 16-18 has been canceled without prejudice or disclaimer to more clearly describe the claimed invention. Further, FIG. 4D has been amended, wherein the boundary between the shallow doped region (304) and the deep doped region (306) has been deleted. Amendments to Claims 10 and 13 are fully supported by FIG. 2E, 4B. It is believed that no new matter adds by way of these amendments made to the claims or specification, or otherwise to the application. For at least for the following reasons, Applicant respectfully submits that claims 10-15 patently define over the prior art of record. Reconsideration is respectfully requested.

Objection to Drawing

The Office Action objected to Drawings because the proposed drawing changes filed on 1-28-2004 are objected to because the proposed changes made to Figure 4D lack an adequate support from the original disclosure. The Examiner states that Applicant intends to separate the shallow doped region 304 from the deeply doped source/drain region 306 in order to support the applicant's assertion that the two regions are formed with two different types of dopants. However, what is shown in FIG. 4D and FIG. 2G are from two different embodiments and viewed from two different dimensions. And, the original disclosure lacks an adequate description regarding the subject matters that the two regions (304 and 306) are distinguishable from each other with a defined boundary therebetween along the defined dimension delined in Fig. 4D and they are formed of two different types of dopants. A drawing correction or corrected drawings are required in reply to the office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

In response thereto, applicants agree that the original disclosure lack support that the shallow doped region (304) and the deep doped region (306) comprise different dopants types. Applicants attach the corrected Drawing as a separate accompanying sheet, wherein the boundary separating the shallow doped region (304) and the deep doped region (306) in FIG. is removed. Accordingly, Applicants would like to request the Examiner to kindly disregard the proposed amendment to FIG. 4D filed on 1-28-2004 and reconsideration the attached proposed amended drawing is respectfully requested.

Objection to Claims

The Office Action objected to claims 10-12 and 17-18 because of the following informalities and/or defects: In claim 10, the terms "said first and second trench profile" lacks sufficient antecedent basis in the claim; and claims 17-18, the term "the thick insulating layer" lacks a sufficient antecedent basis in the claims, as the like term is already deleted from claim 16. Appropriate correction is required.

In response thereto, Applicants have amended claim 10 and canceled claims 17-18. After entry of the above amendments to claim 10, it is believed that the above objections to claims 10-12 and 17-18 can be overcome. Reconsideration is respectfully requested.

Response to Claims Rejections under 35 USC §112

1. The Office Action rejected claims 13-18 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

In rejecting the above claims, the Examiner indicated that claims 13 and 16 recite the subject matter that the deep source/drain regions are doped with dopants of a conductivity type opposite to that in the first and second shallow dopants, but according to the original disclosure, especially in FIG. 4D, the deep doped regions (306) and the shallow regions (304) are of same type, so as to effectively increase the gate width. It is not clear how the device would still be functional if the deep and shallow regions are formed of dopants of different conductivity types.

In response thereto, Applicants would like to thank the Examiner for pointing out the informalities, and accordingly amended FIG. 4D to show the boundary between the shallow doped region 304 and the deep doped region 306. A proposed amended FIG. 4D is attached hereto as a separate accompanying sheet. Reconsideration is respectfully requested.

Response to Claims Rejections under 35 USC§102

The Office Action rejected claims 10, 12, 13, 15, 16 and 18 under 35 U.S.C. 102(b), as being anticipated by Lancaster et al. (US-4,835,584, hereinafter Lancaster).

In rejecting the above claims, the Examiner stated that Lancaster discloses a semiconductor structure (Figure 1-7F, especially figures 4, 5L and/or 7F), comprising a substrate having an active region including a channel region (under each bottom of the gate oxide layer 57 in Fig. 5L or 72 in Fig. 7F) and a non-channel region surrounding the channel

region; a first trench and a second trench disposed near the channel region, a thick insulating layer (57 in Fig. 5L or 72 in Fig. 7F; a silicon oxide gate insulating layer, about 0.1 um, see col. 3, line 61) over the first and second trenches and conformal to the profile of the first and second trenches; a gate electrode (58 in Fig. 5L or 75 in Fig. 7F) disposed over the two trenches and comprising a first vertical portion, a second vertical portion and a horizontal portion, with the first vertical portion being embedded inside and substantially fills the first trench, the second vertical portion being embedded inside and substantially fills the second trench and the horizontal portion being disposed over the substrate and connecting the first and second vertical portions together; a first shallow doped region (the top horizontal portion of the region 73 or 77) within the substrate at an upper corner adjacent to the first vertical portion of the gate electrode and a second shallow region (the upper horizontal portion of region 74 or 78) at an upper corner adjacent to the second vertical portion of the gate electrode; a deep source region (the lower portion of region 73 or 77) and a deep drain region (the lower portion of region 73 or 77) and a deep drain region (the lower portion of region 74 or 78) disposed in a region in the substrate at a depth deeper than the first and second trenches.

Applicants respectfully disagree and would like to point out that anticipation under 35 U.S.C. 102 required each and every elements of the claim in issue must be found in a single cited prior art.

Applicants respectfully submit that independent claims 10 and 13, as amended, are allowable for at least the reason that Lancaster substantially fails to teach, suggest or disclose every features of the claimed invention. More specifically, Lancaster fails to teach, suggest or disclose a MOSFET device comprising at least "a gate electrode disposed over said first and second trenches, the gate electrode comprising a first vertical portion, a second vertical portion and a horizontal portion, wherein the first vertical portion is embedded inside the first trench and said thick insulating layer and [said first vertical portion within the first trench completely fills the first trench], the second vertical portion is embedded inside the second trench and [said thick insulating layer and said second vertical portion within the second trench completely fills

the second trench], and the horizontal portion is disposed over the substrate and connects said first and second vertical portions together as required by the amended claims 10 and 13". The advantage of the above structure is that at least the above gate structure can be fabricated from a more simplified method. Further, the effective width of the gate can be effectively increased by 2nt while at the same time the lateral surface occupation of the gate can also be effectively reduced and thereby allowing increase in the integration of the semiconductor device.

To the contrary, Lancaster substantially discloses (please see FIG. 5H-5J and related disclosure) a semiconductor structure comprising a plurality of trenches formed side by side into the substrate, an insulating layer (57) formed conformal to the trenches (58), a gate electrode (58) formed continuously over the trenches (56) bisecting a pair of trenches (56). The dielectric material (70) is deposited over the vertical portions of the gate electrode (58) which are embedded within the trenches (56). In other words, the insulating layer (57) and the vertical portions of the electrode (58) within the trenches do not completely fill the trenches, instead, Lancaster substantially teaches that the insulating layer (57), the vertical portions of the electrode (58) and the dielectric layer (70) within trenches completely fill the trenches. In other words, Lancaster substantially teaches or discloses besides the vertical portions of the gate electrode (58) and the gate insulating layer (57), an additional dielectric layer (70) completely fill the trenches. Accordingly, Lancaster fails to teach or disclose the insulating layer (57) and the vertical portions of the electrode (58) within the trenches completely fill the trenches as required by the amended claim 10 of the claimed invention. Accordingly, Applicant respectfully submits that Lancaster cannot possibly anticipate Claims 10 and 13 in this regard.

Further, Since Lancaster substantially teaches (FIG. 5G) forming the gate electrode (58)

substantially conformal to sidewalls of the trench, therefore obviously a wider trench would be required. Thus, this would occupy larger lateral space of the substrate and thereby limiting further increase in the integration of semiconductor device.

Furthermore, Applicants respectfully submit that Claims 16-18 are canceled without prejudice or disclaimer and therefore rejections of these claims are now moot.

For at least the foregoing reasons, Applicants respectfully submit Claims 10, 12, 13 and 15 patently define over Lancaster. Reconsideration is respectfully requested.

Response to Claims Rejections under 35 USC§103

The Office Action rejected claims 11, 14 and 17, insofar as being in compliance with 35 U.S.C. 112 and being best understood in view of the claim objections above, under 35 U.S.C. 103(a) as being unpatentable over Lancaster in view of Kimura et al. (US-5,029,321, hereinafter Kimura).

Applicants respectfully disagree and would like to point out that even though the Office Action relied upon Kimura to disclose the thermal oxidation process for forming the gate oxide layer, still Kimura cannot cure the specific deficiencies of the claimed invention for at least the reasons as substantially discussed above. Accordingly, Applicants respectfully submit that Claims 11 and 14 also patently define over Lancaster and Kimura for at least the reasons set forth above. Reconsideration is respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 10-15 are in proper condition for allowance. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted

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